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June 19, 2006

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No.19,572

Subject:	Application No.	:	10/631,841	Confirmation No.:	1036
	Applicant	:	Chun Shiah		
	Filed	:	July 31, 2004		
	Art Unit	:	2816		
	Examiner	:	Long T. Nguyen		
	Docket No.	:	ET01-010C		

APPEAL BRIEF

Dear Sir:

In response to the Final Rejection dated October 11, 2001 of Claims 1-42 under 35 USC §112, first and second paragraphs and under 35 USC §103(a) of the above reference patent application, please accept this appeal brief. The commissioner is hereby authorized to charge payment of $250.00 associated with this communication to Deposit Account No. 19-0033. A duplicate copy of this sheet is enclosed.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

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on 6/21/06 (Date)

Stephen B. Ackerman, Reg. #37,761
Typed or printed name of person signing this certificate

Signature

(i) Real Party in Interest:

An assignment has been recorded for this patent application. The assignee is:

Etron Technologies, Inc.
No. 6 Technology Road 5
Science-Based Industrial Park
Hsin-Chu, Taiwan 30077, R.O.C.

(ii) Related Appeals and Interferences:

There are no related appeals or interferences.

(iii) Status of Claims:

Claims 1-42 have been finally rejected under 35 U.S.C. § 112, first and second paragraphs and under 35 USC §103(a). No claims were allowed.

(iv) Status of Amendments:

Claims 1-42 have not been amended subsequent to Final Rejection. The Examiner states in the Final Rejection that the request for reconsideration of the amendment filed dated October 19, 2005 is still objected to 35 U.S.C. §132 because it introduces new matter into the disclosure of the invention and that claims 1-42 are rejected under 35 USC §112, first paragraph for failing to comply with the written description

requirements; under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention; and under 35 USC §103(a) as being unpatentable over in Applicant's Admitted Prior Art (AAPA) in view of U. S. Patent 6,373,328 (Rapp) .

(v) Summary of the Invention:

Briefly, the applicants wish to point out the major features of their invention, which is a novel low jitter input buffer with small input signal swing. The low jitter input buffer includes a buffer input portion **101** of Fig. 2 and a buffer output portion **201** of Fig. 2. The buffer input portion **101** is constructed of the NMOS transistors **N11** and **N12** of Fig. 2 and PMOS transistors **P11** and **P12** of Fig. 2. The lower supply voltage **VSS** is applied to the source nodes of the NMOS transistors **N11** and **N12** of Fig. 2 and an upper supply voltage **VDD** is applied to the source nodes of the PMOS transistors **P11** and **P12** of Fig. 2. The gate nodes of transistors **P11** and **P12** and the drains of transistors **N11** and **P11** are connected together to form the biasing node **b11** of Fig. 2. The biasing voltage **VB11** is developed at the biasing node **b11** as a result of the configuration of transistors **P11** and **P12**. A parasitic capacitor **Cp** of Fig. 2 is inherently coupled from the biasing node **b11** to the ground reference node. A reference supply voltage **VREF** is applied to the gate of transistor **N11**, input signal SIGNAL_IN is applied to the gate of **N12**. A large capacitor

CHC is attached between the bias node **b11** and the lower supply voltage **VSS**. The buffer output portion **201** of Fig. 2 includes a common node for the drain of NMOS transistor **N12** and the drain of PMOS transistor **P12**, which serves as input to inverter of Fig. 2. The output of inverter **I11** of Fig. 2 is the output signal **SIGNAL_OUT1** of Fig. 2.

The large capacitance **CHC** is in series with the parasitic capacitor **Cp** of the input buffer receiver transistors **N11**, **P11**, and **P12**. The large capacitor **CHC**, as connected, is designed to have an extremely large capacitance relative to the parasitic capacitor **Cp** such that the bias voltage **VB11** essentially follows the voltage changes in the lower supply voltage **VSS** preventing the effects of the **VSS** noise. This coupling ratio is determined by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor CHC.

Cp is the capacitance value of the parasitic capacitor Cp.

Because of its large coupling ratio (very close to 1), the capacitor **CHC** essentially charge couples the biasing voltage **VB11** at the bias node **b11**, to the lower supply voltage **VSS**, of devices **N11** and **N12**. This

forces the transistors **N11** and **N12** to activate and deactivate essentially simultaneously, allowing for a quicker response time on output signal **SIGNAL_OUT1**.

Claims 1, 12, 23, and 33 are read on the specification and drawings as follows:

1. An input buffer receiver comprising:

a buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2) for receiving an input signal (**SIGNAL_IN** of Fig. 2; paragraph [**0017**], Line 13), said buffer input portion (**b1** of Fig. 2; paragraph [**0017**], Line 8) comprising a bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8);

a large capacitor (**CHC** of Fig. 2; paragraph [**0017**], Line 7) coupled between the bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8) and a lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) for providing a coupling ratio between a capacitance value of said large capacitor (**CHC** of Fig. 2; paragraph [**0017**], Line 7) and a capacitance value of a parasitic capacitor (**Cp** of Fig. 2; paragraph [**0017**], Line 10) coupled between said bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8) and a ground reference point is approximately equal to a unity value such that a biasing

voltage (**Vb11** in paragraph [**0017**], Line 8) at said biasing node (**b1** of Fig. 2; paragraph [**0017**], Line 8) follows said lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) to minimize effects of a ground noise signal between the lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) and the ground reference point; and

a buffer output portion (**201** of Fig. 2; paragraph [**0017**], Line 2) in communication with the buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2) for producing an output signal (**SIGNAL_OUT1** of Fig. 2; paragraph [**0017**], Line 17).

12. An integrated circuit formed on a substrate comprising:

an input buffer receiver for receiving an input signal, said input buffer comprising:

a buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2) for receiving an input signal **SIGNAL_IN** of Fig. 2; paragraph [**0017**], Line 13), said buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2) comprising a bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8);

a large capacitor (**CHC** of Fig. 2; paragraph [**0017**], Line 7) coupled between the bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8) and a lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) for providing a coupling ratio between a capacitance value of said large capacitor (**CHC** of Fig. 2; paragraph [**0017**], Line 7) and a capacitance value of a parasitic capacitor (**Cp** of Fig. 2; paragraph [**0017**], Line 10) coupled between said bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8) and a ground reference point is approximately equal to a unity value such that a biasing voltage (**Vb11** in paragraph [**0017**], Line 8) at said biasing node (**b1** of Fig. 2; paragraph [**0017**], Line 8) follows said lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) to minimize effects of a ground noise signal between the lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) and the ground reference point; and

a buffer output portion (**201** of Fig. 2; paragraph [**0017**], Line 2) in communication with the buffer

input portion (**201** of Fig. 2; paragraph [**0017**], Line 2) for producing an output signal(**SIGNAL_OUT1** of Fig. 2; paragraph [**0017**], Line 17).

23. A method for minimizing effects of ground noise on an input buffer receiver comprising the steps of:

forming a buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2) for receiving an input signal **SIGNAL_IN** of Fig. 2; paragraph [**0017**], Line 13) on a substrate;

forming a bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8) within said buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2);

connecting a lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) to said buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2);

forming a large capacitor (**CHC** of Fig. 2; paragraph [**0017**], Line 7) coupled between the bias node and the lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) for providing a coupling ratio between a capacitance value of said large capacitor (**CHC** of Fig. 2; paragraph [**0017**], Line 7) and a capacitance value of a parasitic

capacitor (**Cp** of Fig. 2; paragraph **[0017]**, Line 10) coupled between said bias node (**b1** of Fig. 2; paragraph **[0017]**, Line 8) and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node (**b1** of Fig. 2; paragraph **[0017]**, Line 8) follows said lower supply voltage (**VSS** of Fig. 2; paragraph **[0017]**, Line 10) to minimize effects of said ground noise between the lower supply voltage (**VSS** of Fig. 2; paragraph **[0017]**, Line 10) and the ground reference point; and

forming a buffer output portion (**201** of Fig. 2; paragraph **[0017]**, Line 2) on said substrate in communication with the buffer input portion (**101** of Fig. 2; paragraph **[0017]**, Line 2) for producing an output signal.

33. An apparatus for minimizing effects of ground noise within an input buffer receiver, said apparatus comprising:

means for forming a buffer input portion (**101** of Fig. 2; paragraph **[0017]**, Line 2) for receiving an input signal **SIGNAL_IN** of Fig. 2; paragraph **[0017]**, Line 13) on a substrate;

means for forming a bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8) within said buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2);

means for connecting a lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) to said buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2);

means for forming a large capacitor (**CHC** of Fig. 2; paragraph [**0017**], Line 7) between the bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8) and the lower supply voltage (**VSS** of Fig. 2; paragraph [**0017**], Line 10) for providing a coupling ratio between a capacitance value of said large capacitor (**CHC** of Fig. 2; paragraph [**0017**], Line 7) and a capacitance value of a parasitic capacitor (**Cp** of Fig. 2; paragraph [**0017**], Line 10) coupled between said bias node (**b1** of Fig. 2; paragraph [**0017**], Line 8) and a ground reference point is approximately equal to a unity value such that a biasing voltage (**Vb11** in paragraph [**0017**], Line 8) at said biasing node (**b1** of Fig. 2; paragraph [**0017**], Line 8) follows said lower supply voltage (**VSS** of Fig. 2) to minimize effects of said

ground noise between the lower supply voltage (**VSS** of Fig. 2) and the ground reference point; and

means for forming a buffer output portion (**201** of Fig. 2; paragraph [**0017**], Line 2) on said substrate in communication with the buffer input portion (**101** of Fig. 2; paragraph [**0017**], Line 2)for producing an output signal.

(vi) Grounds of rejection to be reviewed on appeal:

The issues of this appeal are whether:

1) The amendment filed 1/14/05 should be objected to under 35 U.S.C. §132 because it introduces new matter into the disclosure of the invention;

2) Claims 1-42 are unpatentable under 35 USC §112, first paragraph for failing to comply with the written description requirements; and

3) Claims 1-42 are unpatentable under 35 USC §103(a) of Claims 1-42 over in Applicant's Admitted Prior Art (AAPA) in view of U. S. Patent 6,373,328 (Rapp)

(vii) Argument:

Reconsideration of the objection to the amendment filed 1/14/05 under 35 U.S.C. §132 because it introduces new matter into the disclosure of the invention. The applicant believes that added material is not new matter. The original text describes that:

"Because of its large coupling ratio, CHC essentially charge couples the VB11 gate voltage of the PMOS bias node, to the VSS source voltage..." (Page 5, last paragraph, lines 2-4)

Employing basic electronic principles, the large coupling ratio provides a charge coupling or AC coupling of the biasing voltage VB11 at the bias node b11 to the lower supply voltage VSS. Thus the coupling ratio would be defined as:

$$CR = \frac{VB11}{VSS} = \frac{VSS\dfrac{Z_{CP}}{Z_{HC}+Z_{CP}}}{VSS} = \frac{Z_{CP}}{Z_{HC}+Z_{CP}}$$

$$= \frac{\dfrac{1}{j\omega C_P}}{\dfrac{1}{j\omega C_{HC}}+\dfrac{1}{J\omega C_{HC}}} = \frac{C_{HC}}{C_{HC}+C_P}$$

Where:

$$Z_{CP} = \frac{1}{j\omega C_P},$$

$$Z_{HC} = \frac{1}{J\omega C_{HC}}, \text{ and}$$

$$VB11 = V_{CP} = VSS\frac{Z_{CP}}{Z_{HC}+Z_{CP}}.$$

It can be shown that as the magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P grows larger, any noise voltage present on the lower supply voltage VSS is charge coupled or AC coupled directly to the bias node **b11**. Further it is apparent that the larger magnitude of the capacitance of the large

capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P, the coupling ratio approaches a maximum value of unity (1), therefore a large coupling value would clearly be any value that approached unity (1).

Reconsideration of the rejection under 35 USC §112, first paragraph of Claims 1-42 for failing to comply with the written description requirements, in that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor at the time of the application was filed, had possession of the claimed invention is requested in light of the following arguments.

The original text describes that:

> "Because of its large coupling ratio, CHC essentially charge couples the VB11 gate voltage of the PMOS bias node, to the VSS source voltage..." (Page 5, last paragraph, lines 2-4)

Employing basic electronic principles, the large coupling ratio provides a charge coupling or AC coupling of the biasing voltage VB11 at the bias node b11 to the lower supply voltage VSS. Thus the coupling ratio would be defined:

$$CR = \frac{VB11}{VSS} = \frac{VSS\dfrac{Z_{CP}}{Z_{HC}+Z_{CP}}}{VSS} = \frac{Z_{CP}}{Z_{HC}+Z_{CP}}$$

$$= \frac{\dfrac{1}{j\omega C_P}}{\dfrac{1}{j\omega C_{HC}}+\dfrac{1}{j\omega C_{HC}}} = \frac{C_{HC}}{C_{HC}+C_P}$$

Where:

$Z_{CP} = \dfrac{1}{j\omega C_P}$ is the impedance of the parasitic capacitance C_P.

$Z_{HC} = \dfrac{1}{j\omega C_{HC}}$ is the impedance of the very large capacitance C_{HC}.

$VB11 = V_{CP} = VSS\dfrac{Z_{CP}}{Z_{HC}+Z_{CP}}$ is the voltage VB11 present at the node b11 and can be found as a voltage divider of the impedance Z_{HC} of the very large capacitor C_{HC} and the impedance Z_{CP} of the parasitic capacitor C_P as shown.

It can be shown that as the magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P grows larger, any noise voltage present on the lower supply voltage VSS

is charge coupled or AC coupled directly to the bias node b11. Further it is apparent that the larger magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P, the coupling ratio approaches a maximum value of unity (1), therefore a large coupling value would clearly be any value that approached unity (1).

The concept of coupling ratio is not new in the art, as shown in Silicon Processing for the VLSI Era, Volume II Process Integration, Wolf, Latice Press, Sunset Beach, CA., 1990, pp: 623-627. In nonvolatile or Flash memory, the capacitive coupling coefficient of the capacitance of the control gate to the floating gate of the nonvolatile memory cell and the capacitance of the floating gate of the nonvolatile memory cells to the bulk semiconductor substrate of a nonvolatile memory cell, the coupling coefficient is used to determine the amount of charge coupled to the floating gate to determine the necessary programming voltages and the time for programming the nonvolatile memory cell. The serial structure of the floating gate nonvolatile memory employs similar concepts to the present invention. The very large capacitor C_{HC} in series with the parasitic capacitor C_P as shown in Fig. 4a demonstrates that the large value of capacitance of the very large capacitor C_{HC} relative to the parasitic capacitor C_P causes the voltage VB11 at the node b11 is essentially equal to the lower supply voltage VSS and the coupling ratio approaches one (1) as shown above.

Reconsideration of the rejection under 35 USC §112, second paragraph, of Claims 1-42 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention is requested in light of the following arguments.

In Claims 1, 12, 23, and 33, a large capacitor is coupled between the bias node and the lower supply voltage:

> "for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point."

As shown in Silicon Processing for the VLSI Era, Volume II Process Integration, Wolf, Latice Press, Sunset Beach, CA., 1990, pp: 623-627, the coupling ratio is not the ratio of the value of capacitance between the very large capacitor C_{HC} and parasitic capacitor C_P (C_{HC}/C_P), but the AC coupling of the biasing voltage VB11 at the bias node b11 to the lower supply voltage VSS. This is essentially a capacitive voltage divider and as

shown above, the voltage VB11 at the bias node b11 become a function of the coupling ratio ($\frac{C_{HC}}{C_{HC}+C_P}$).

Reconsideration of the rejection under 35 USC §103(a) of Claims 1-42 as being unpatentable over in Applicant's Admitted Prior Art (AAPA) in view of U. S. Patent 6,373,328 (Rapp) is requested in light of the following arguments.

The AAPA does illustrate an input buffer receiver and Rapp does show "an n-type transistor 90" connected to serve "as a capacitor, helping to hold the voltage constant at the gate of transistor 86" (Rapp, Col 9, Lines 38-42). Neither AAPA, nor Rapp, nor AAPA in combination with Rapp include:

> a large capacitor between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point; (Claim 1, Lines 4-11 and Claim 12, Lines 7-17)

forming a large capacitor between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point; (Claim 23, Lines 6-13)

and

means for forming a large capacitor between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point. (Claim 33, Lines 8-15)

The large capacitor in Rapp is connected to the ground reference point and does not charge couple the biasing node to the lower supply voltage such that the voltage at the biasing node follows the lower supply

voltage. Further, the circuit of Rapp provides a comparator circuit that compares the voltage value of a programming voltage supply V_{PP} at node A of Fig. 5 of Rapp against the voltage value of the power supply voltage V_{DD}. The capacitor of Rapp helps "to hold the voltage constant at the gate of transistor 86" this does not provide the coupling of the lower supply voltage to the biasing node of this invention.

The invention as claimed in amended Claims 1-42 is believed to be novel and patentable over AAPA in view of Rapp because there is not sufficient basis for concluding that claimed elements of either AAPA, or Rapp, or AAPA in combination with Rapp would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. The applicant believes that there is no such basis for the combination.

(viii) Claims appendix.

Listing of Claims:

1. An input buffer receiver comprising:

a buffer input portion for receiving an input signal, said buffer input portion comprising a bias node;

a large capacitor coupled between the bias node and a lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

2. The input buffer receiver of claim 1, wherein the buffer input portion which receives the input signal further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which the input signal is applied, and a drain node which is coupled to the drain of a fourth transistor and to an input node of the buffer output portion.

3. The input buffer receiver of claim 2, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

4. The input buffer receiver of claim 2, wherein the large capacitor is connected between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

5. The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to its drain.

6. The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to the drain of the first transistor.

7. The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to the gate of the third transistor.

8. The input buffer receiver of claim 2, wherein the buffer output portion which produces the output signal comprises: a first inverter connected to the drain of the third transistor and the drain of the fourth transistor.

9. The input buffer receiver of claim 2, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

10. The input buffer receiver of claim 1, wherein the large capacitor charge couples the bias node of the input buffer receiver to the

lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

11. The input buffer receiver of claim 1, wherein the capacitance value of the large capacitor is chosen to be very large with respect to said capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

12. An integrated circuit formed on a substrate comprising:

an input buffer receiver for receiving an input signal, said input buffer comprising:

a buffer input portion for receiving the input signal, said buffer input portion comprising a bias node;

a large capacitor coupled between the bias node and a lower supply voltage for providing a coupling

ratio between a capacitance value said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point ; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

13. The integrated circuit of claim 12, wherein the buffer input portion of the input buffer receiver further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is

developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which an input signal is applied, and a drain node which is connected to the drain of a fourth transistor and to an input node of the buffer output portion.

14. The integrated circuit of claim 13, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

15. The integrated circuit of claim 13, wherein the large capacitor is connected between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

16. The integrated circuit of claim 13, wherein the gate of the second transistor is connected to its drain.

17. The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the drain of the first transistor.

18. The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the gate of the third transistor.

19. The integrated circuit of claim 13, wherein the buffer output portion which produces said output signal comprises: a first inverter connected to the drain of the third transistor and the drain of the fourth transistor.

20. The integrated circuit of claim 13, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

21. The integrated circuit of claim 12, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

22. The integrated circuit of claim 12, wherein the capacitance value of the large capacitor is chosen to be very large with respect to said capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

23. A method for minimizing effects of ground noise on an input buffer receiver comprising the steps of:

forming a buffer input portion for receiving an input signal on a substrate;

forming a bias node within said buffer input portion;

connecting a lower supply voltage to said buffer input portion;

forming a large capacitor coupled between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply

voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point; and

forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

24. The method of claim 23, wherein forming the buffer input portion further comprises the steps of:

forming a first transistor of a first conductivity type on said substrate;

applying the lower supply voltage to a source node of the first transistor;

applying a reference voltage to a gate node of the first transistor;

connecting a drain node of the first transistor to develop a biasing voltage at said drain node;

forming a second transistor of a second conductivity type on said substrate;

connecting a drain node of the second transistor to the drain node of the first transistor;

connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

connecting a source node of the second transistor to an upper supply voltage;

forming a third transistor of the second conductivity type on said substrate;

connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

connecting a source node of the third transistor to the upper supply voltage source;

forming a fourth transistor of the first conductivity type on said substrate;

connecting a source node of the fourth transistor to the lower supply voltage;

connecting a gate node of the fourth transistor to receive an input signal; and

connecting a drain node of the fourth transistor to a drain node of the third transistor and to an input node of the buffer output portion.

25. The method of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

26. The method of claim 24, wherein forming the large capacitor comprises the step of:

connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

27. The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to its drain.

28. The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to the gate of the third transistor.

29. The method of claim 24, wherein forming the buffer output portion which produces the output signal comprises the step of:

forming a first inverter on said substrate; and

connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor.

30. The method of claim 24, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

31. The method of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

32. The method of claim 23, wherein the capacitance value of the large capacitor is chosen to be very large with respect to said capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

33. An apparatus for minimizing effects of ground noise within an input buffer receiver, said apparatus comprising:

means for forming a buffer input portion for receiving an input signal on a substrate;

means for forming a bias node within said buffer input portion;

means for connecting a lower supply voltage to said buffer input portion;

means for forming a large capacitor between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point; and

means for forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

34. The apparatus of claim 33, wherein forming the buffer input portion further comprises:

means for forming a first transistor of a first conductivity type on said substrate;

means for applying the lower supply voltage to a source node of the first transistor;

means for applying a reference voltage to a gate node of the first transistor;

means for connecting a drain node of the first transistor to develop as biasing voltage at said drain node;

means for forming a second transistor of a second conductivity type on said substrate;

means for connecting a drain node of the second transistor to the drain node of the first transistor;

means for connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

means for connecting a source node of the second transistor to an upper supply voltage;

means for forming a third transistor of the second conductivity type on said substrate;

means for connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

means for connecting a source node of the third transistor to the upper supply voltage source;

means for forming a fourth transistor of the first conductivity type on said substrate;

means for connecting a source node of the fourth transistor to the lower supply voltage;

means for connecting a gate node of the fourth transistor to receive said input signal; and

connecting a drain node of the fourth transistor to a drain node of the third transistor and to an input of the buffer output portion.

35. The apparatus of claim 34, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

36. The apparatus of claim 34, wherein means for forming the large capacitor comprises:

means for connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

37. The apparatus of claim 34, wherein means for forming the buffer input portion further comprises:

means for connecting the gate of the second transistor to its drain.

38. The apparatus of claim 34, wherein means for forming the buffer input portion further comprises the steps of:

means for connecting the gate of the second transistor to the gate of the third transistor.

39. The apparatus of claim 34, wherein means for forming the buffer output portion which produces said output signal comprises:

means for forming a first inverter on said substrate; and

means for connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor.

40. The apparatus of claim 34, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

41. The apparatus of claim 33, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor **CHC**, and

Cp is the capacitance value of the parasitic capacitor **Cp**.

42. The apparatus of claim 33, wherein the capacitance value of the large capacitor is chosen to be very large with respect to said capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

(ix) Evidence appendix.

There is no evidence submitted pursuant to 37 CFR §§ 1.130, 1.131, or 1.132 or any other.

(x) Related proceedings appendix.

There are no related appeals or interferences.

The applicants request that the Board of Appeals reverse the holding of the examiner in finally rejecting the Claims of the application. Allowance of all Claims is requested.

Respectfully Submitted,
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